Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application. In this listing, claim 12 is cancelled and new claims 16-18 are added for consideration. Now, claims 1-11 and 13-18 are pending in this application.

1. (Currently Amended) A system comprising:

a plurality of functional devices accessing a memory bus wherein said memory bus allows access by one of said functional devices for one cycle of period of time;

a plurality of request agents corresponding to said functional devices;

a control register respectively storing access priority grades for said request agents;

a plurality of counter timers respectively loading said access priority grades; and

a bus elector coupled with said counter timers, wherein said bus elector respectively compares said loaded access priority grades and elects one out of said request agents according to said compared access priority grades;

wherein said memory bus allows access by one of said functional devices corresponding to said elected request agent for one cycle of period of time; and

wherein one or more of said access priority grades loaded in said counter timers are timely updated on a clock cycle basis.

2. (Original) The system of claim 1 wherein said functional devices are selected from the group consisting of memory controllers, image processors, motion estimation processors, host and peripheral interfaces.

3. (Currently Amended) The system of claim 1 wherein said access priority grades are counter values ranging from a greatest value ~~largest~~ to a smallest value and said elected request agent ~~is one that includes~~ corresponds to the smallest counter value.

4. (Currently Amended) The system of claim 1 wherein said access priority grades are counter values ranging from a greatest value ~~largest~~ to a smallest value and said elected request agent ~~is one that includes~~ corresponds to the ~~largest~~ greatest counter value.

5. (Currently Amended) The system of claim 1 further comprising a control unit ~~for~~ connected to said request agents for respectively receiving corresponding requests for access to said memory bus.

6. (Currently Amended) A memory bus arbiter for a system having a plurality of functional devices accessing a memory bus with a plurality of request agents corresponding to the functional devices, the memory bus arbiter comprising:

a control register respectively storing access priority grades for said request agents;

a plurality of counter timers respectively loading said access priority grades; and

a bus elector coupled with said counter timers, wherein said bus elector respectively compares said loaded access priority grades and elects one out of said request agents according to said compared access priority grades;

wherein said memory bus allows access by one of said functional devices corresponding to said elected request agent for one cycle of period of time; and

wherein one or more of said access priority grades loaded in said counter timers are timely updated on a clock cycle basis.

7. (Original) The memory bus arbiter of claim 6 wherein said functional devices are selected from the group consisting of memory controllers, image processors, motion estimation processors, host and peripheral interfaces.

8. (Currently Amended) The memory bus arbiter of claim 6 wherein said access priority grades are counter values ranging from a greatest value ~~largest~~ to a smallest value and said elected request agent ~~is one that includes~~ corresponds to the smallest counter value.

9. (Currently Amended) The memory bus arbiter of claim 6 wherein said access priority grades are counter values ranging from a greatest value ~~largest~~ to a smallest value and said elected request agent ~~is one that includes~~ corresponds to the ~~largest~~ greatest counter value.

10. (Currently Amended) The memory bus arbiter of claim 6 further comprising a control unit ~~for~~ connected to said request agents for respectively receiving corresponding requests for access to said memory bus.

11. (Currently Amended) A method for a system having a plurality of functional devices accessing a memory bus, the method comprising ~~the steps of~~:

~~(a)~~ providing a plurality of request agents respectively corresponding to said functional devices;

~~(b)~~ storing access priority grades for said request agents in a plurality of counter timers;

~~(c)~~ comparing said access priority grades;

~~(d)~~ electing a request agent out of said request agents according to said compared access priority grades; ~~and~~

~~(e)~~ allowing access to said memory bus for one cycle of period of time by one of said functional devices corresponding to said elected request agent to said memory bus; and

updating one or more of said access priority grades based on a clock cycle.

12. (Cancelled)

13. (Currently Amended) The method of claim 11 wherein said access priority grades are counter values ranging from a greatest value ~~largest~~ to a smallest value and said elected request agent ~~is one that includes~~ corresponds to the smallest counter value.

14. (Currently Amended) The method of claim 11 wherein said access priority grades are counter values ranging from a greatest value ~~largest~~ to a smallest value and said elected request agent ~~is one that includes~~ corresponds to the ~~largest~~ greatest counter value.

15. (Original) The method of claim 11 wherein said functional devices are selected from the group consisting of memory controllers, image processors, motion estimation processors, host and peripheral interfaces.

16. (New) The method of claim 11 wherein updating said access priority grades stored in said counter timers includes decreasing one or more of said access priority grade values by a value of 1.

17. (New) The system of claim 1 wherein one or more of said access priority grade values loaded in said counter timers are timely decreased by a value of 1.

18. (New) The memory bus arbiter of claim 6 wherein one or more of said access priority grade values loaded in said counter timers are timely decreased by a value of 1.